IN THE DRAWINGS

Applicants propose to label the blocks in Figs. 1-3 and to revise Fig. 1 in accordance with the accompanying ANNOTSTED SHEETS SHOWING CHANGES.

Enclosed herewith are REPLACEMENT SHEETS in which the above changes have been incorporated.

REMARKS

The claims have been amended to more clearly define the invention as disclosed in the written description. In particular, the claims have been amended for clarity.

The Examiner has rejected claims 1, 2 and 7-10 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,157,492 to Tults. The Examiner has further rejected claims 3-6 under 35 U.S.C. 103(a) as being unpatentable over Tults.

The Tults patent discloses sync validity detecting utilizing a microcomputer, in which, in reference to Fig. 1 therrein, a microcomputer-controlled tuning system is described, including a tuner, a microcomputer and a stage for receiving tuned signals from the tuner.

As noted in MPEP §2131, it is well-founded that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond,* 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The subject invention, as claimed in claim 1, includes the limitation "said stage comprises a phase-locked-loop coupled to receive said tuned signals, said phase-locked loop generating a lock signal when locked to said tuned signals, said lock signal forming said at least one control signal for said controller".

Applicants submit that this limitation is neither shown nor suggested by Tults. In particular, while Tults shows a phase-locked loop 115, it should be noted that PLL 115 does not receive the tuned signals. Rather, PLL 115 "generates a tuning voltage (TV) in response to an error produced by comparing the frequency (and phase) of a signal derived by dividing the frequency of the local oscillator (LO) signal by a controllable division factor N to a reference frequency signal. Division factor N is controlled by a microcomputer (μC) 117,..." (col. 2, lines 52-58).

Applicants submit that the PLL 115 of Tults is equivalent to the phase-locked loop 13-17 shown in Fig. 1 of the subject application. However, this is not the phase-locked loop being referred to in the claim. Rather, the "stage" referred to in claim 1 is the IF stage 3 of Fig. 1, and the phase-locked loop as claimed is the PLL 31 shown in Fig. 1. As shown in Fig. 1, and described in the specification on page 4, lines 22-33, this PLL 31 receives the tuned signals and applies a lock signal 53 to the controller 2.

Applicants further submit that this difference is significant in the PLL 31 is able to generate a lock signal much

more quickly than the automatic fine tuning circuit 32 is able to appropriately tune to the signals tuned to by the tuner 1.

In view of the above, Applicants believe that the subject invention, as claimed, is neither anticipated nor rendered obvious by the prior art, and as such, is patentable thereover.

Applicants believe that this application, containing claims 1-10, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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